

What Is Claimed Is:

1. A high electron mobility transistor using a Group III-V compound semiconductor, comprising
 - 5 an undoped second channel layer laminated on an InP substrate via a buffer layer;
 - an undoped first channel layer laminated on said second channel layer; and
 - a doped electron-supplying layer laminated on
- 10 said first channel layer,
 - wherein said first channel layer is composed of $In_{1-x}Ga_xAs$ and has an energy level of conduction band lower than that of said electron-supplying layer,
 - said second channel layer is composed of a Group
- 15 III-V compound semiconductor using a Group V element other than P, has an energy level of conduction band higher than that of the first channel layer, and has a band gap wider than that of the first channel layer.
- 20 2. The high electron mobility transistor as described in claim 1, wherein said first and second channel layers are formed to have a thickness small enough to have discrete quantum levels, a first quantum level being formed only in the first channel layer, and a second
- 25 quantum level being formed in both the first and second channel layers.

3. The high electron mobility transistor as described in claim 1 or claim 2, wherein said electron-supplying layer is composed of $\text{In}_{1-y}\text{Al}_y\text{As}$, the first channel layer is composed of $\text{In}_{1-x}\text{Ga}_x\text{As}$, and the second 5 channel layer is composed of $\text{In}_{1-x}(\text{Al}_{1-z}\text{Ga}_z)_x\text{As}$.

4. The high electron mobility transistor as described in claim 1 or claim 2, wherein said electron-supplying layer is composed of $\text{In}_{1-y}\text{Al}_y\text{As}$, the first 10 channel layer is composed of $\text{In}_{1-x}\text{Ga}_x\text{As}$, and the second channel layer is composed of $\text{In}_{1-x}(\text{Al}_{1-z}\text{Ga}_z)_x(\text{As}_{1-z_2}\text{Sb}_{z_2})$.

5. The high electron mobility transistor as described in claim 3 or claim 4, wherein the thickness of 15 said first channel layer is 3~7 nm.

6. The high electron mobility transistor as described in claim 3 or claim 4, wherein the thickness of said second channel layer is 10~20 nm.

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7. The high electron mobility transistor as described in claim 3 or claim 4, wherein the composition ratio (1-z) of Al element in said second channel layer is 0.05~0.5.

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8. The high electron mobility transistor as described in claim 1 or claim 2, wherein said electron-

supplying layer is composed of $In_{1-y}Al_yAs$, the first channel layer is composed of $In_{1-x}Ga_xAs$, and the second channel layer is composed of $In_{1-x}Ga_xAs$ with the In composition ratio lower and the gallium composition ratio 5 higher than those in the first channel layer.

9. The high electron mobility transistor as described in claim 1 or claim 2, wherein an element separation groove is formed which extends from said 10 electron-supplying layer to said buffer layer.

10. A high electron mobility transistor using a Group III-V compound semiconductor, comprising an undoped second channel layer laminated on an 15 InP substrate via a buffer layer and composed of $In_{1-x}(Al_{1-z}Ga_z)_xAs$ (where the composition ratio (z-1) of Al is 0.05-0.5) which is lattice matched to InP, an undoped first channel layer laminated on said second channel layer and composed of $In_{1-x}Ga_xAs$ which is 20 lattice matched to InP, and a doped electron-supplying layer laminated on said first channel layer and composed of $In_{1-y}Al_yAs$ which is lattice matched to InP.

25 11. The high electron mobility transistor as described in claim 10, wherein said first and second channel layers are formed to have a thickness small enough

to have the discrete quantum levels, a first quantum level being formed only in the first channel layer, and a second quantum level being formed in both the first and second channel layers.

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